AMENDMENTS TO THE CLAIMS

Claims 1-27 (Cancelled)

28. (Currently Amended) A semiconductor device comprising:

a die having:

a semiconductor structure that includes a substrate and a plurality of devices that are formed in and on the substrate; and

an interconnect structure connected to the semiconductor structure to electrically interconnect the devices to realize a circuit, the interconnect structure having a top surface, a dielectric structure, and a metal trace that contacts the dielectric structure; and

~~a test~~ an external structure that contacts the top surface;

a first opening formed in the dielectric structure, the first opening extending from the top surface down to a first region of the metal trace;

a first conductive structure formed in the first opening to electrically connect the first region of the metal trace and the ~~test~~ external structure;

a second opening formed in the dielectric structure, the second opening extending from the top surface down to a second region of the metal trace;

a second conductive structure formed in the second opening to electrically connect the second region of the metal trace and the ~~test~~ external structure; and

a third opening formed in the dielectric structure, the third opening extending from the top surface down through the metal trace to break an electrical connection between the first and second regions of the metal trace.

Claims 29-34 (Cancelled)

35. (Currently Amended) The semiconductor device of claim 28 wherein the ~~test device~~ external structure includes a first conductive region having a first surface adhered to an exterior surface of the interconnect structure and an opposing second surface.

36. (Currently Amended) The semiconductor device of claim 35 wherein the ~~test device~~ external structure includes an insulation region having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region.

37. (Currently Amended) The semiconductor device of claim 36 wherein the ~~test device~~ external structure includes a second conductive region having a first surface and an opposing second surface, the first surface of the second conductive region contacting the second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region.

38. (Previously Presented) A semiconductor device comprising:

a die having:

a semiconductor structure that includes a substrate and a plurality of devices that are formed in and on the substrate; and

an interconnect structure connected to the semiconductor structure to electrically interconnect the devices to realize a circuit, the interconnect structure having a top surface, a number of bond pads, a dielectric structure that contacts the bond pads, a first metal region that contacts the dielectric structure, and a second metal region that contacts the dielectric structure; and

a region of silicon having a bottom surface connected to only a non-conductive region of the top surface of the interconnect structure, and being spaced apart from the bond pads.

39. (Previously Presented) The semiconductor device of claim 38 and further comprising:

a first opening formed in the dielectric structure, the first opening extending from the top surface down to the first metal region; and

a first conductive structure formed in the first opening, the first conductive structure being electrically connected to the first metal region and the region of silicon.

40. (Previously Presented) The semiconductor device of claim 39 and further comprising:

a second opening formed in the dielectric structure, the second opening extending from the top surface down to the second metal region; and

a second conductive structure formed in the second opening, the second conductive region being electrically connected to the second metal region and the region of silicon, the first and second conductive structures being spaced apart.

41. (Previously Presented) The semiconductor device of claim 40 and further comprising a third opening formed in the dielectric structure, the third opening extending down from the top surface to break an electrical connection between the first and second metal regions.

42. (Previously Presented) The semiconductor device of claim 39 and further comprising:

a dielectric region formed to contact the region of silicon;

a conductor region formed to contact the dielectric region, the conductor region being electrically isolated from the region of silicon;

a second opening formed in the dielectric structure, the second opening extending from the top surface down to the second metal region; and

a second conductive structure formed in the second opening, the second conductive structure being electrically connected to the second metal region and the region of silicon, the first and second conductive structures being spaced apart.

43. (Previously Presented) The semiconductor device of claim 42 and further comprising a third opening formed in the dielectric structure, the third opening extending down from the top surface to break an electrical connection between the first and second metal regions.

44. (Previously Presented) The semiconductor device of claim 38 wherein the region of silicon has a concentration of dopant atoms.

45. (Previously Presented) The semiconductor device of claim 44 and further comprising:

a first opening formed in the dielectric structure, the first opening extending from the top surface down to the first metal region; and

a first conductive structure formed in the first opening, the first conductive structure being electrically connected to the first metal region and the region of silicon.

46. (Previously Presented) The semiconductor device of claim 45 and further comprising:

a second opening formed in the dielectric structure, the second opening extending from the top surface down to the second metal region; and

a second conductive structure formed in the second opening, the second conductive structure being electrically connected to the second metal region and the region of silicon, the first and second conductive structures being spaced apart.

47. (Previously Presented) The semiconductor device of claim 46 and further comprising a third opening formed in the dielectric structure, the third opening extending down from the top surface to break an electrical connection between the first and second metal regions.

48. (Previously Presented) The semiconductor device of claim 44 and further comprising:

a dielectric region formed to contact the region of silicon; and

a conductor region formed to contact the dielectric region, the conductor region being electrically isolated from the region of silicon.

49. (Previously Presented) The semiconductor device of claim 48 and further comprising:

a second opening formed in the dielectric structure, the second opening extending from the top surface down to a second metal region; and

a second conductive structure formed in the second opening, the second conductive structure being electrically connected to the second metal region and the conductor region, the first and second conductive structures being spaced apart.

50. (Previously Presented) The semiconductor device of claim 49 and further comprising a third opening formed in the dielectric structure, the third opening extending down from the top surface to break an electrical connection between the first and second metal regions.

51. (Cancelled)